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Sheet 1 of 4

MySrsForm PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-2506	PRIORITY SERIAL NO. 10/364,710
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Arup Bhattacharyya	
				PRIORITY FILING DATE February 10, 2003	GROUP 2814 Unknown
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	AB		Yamauchi, N. et al., "Drastically Improved Performance in Poly-Si TFTs with Channel Dimensions Comparable to Grain Size", IEDM Tech. Digest, 1989, pp. 353-356.		
	AC		King, T. et al., "A Low-Temperature ( $\leq 550^\circ\text{C}$ ) Silicon-Germanium MOS Thin-Film Transistor Technology for Large-Area Electronics", IEDM Tech. Digest, 1991, pp. 567-570.		
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	AE		Jeon, J. et al., "A New Poly-Si TFT with Selectively Doped Channel Fabricated by Novel Excimer Laser Annealing", IEDM Tech. Digest, 2000, pp. 213-216.		
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	AI		Jagar, S. et al., "Single Grain Thin-Film-Transistor (TFT) with SOI CMOS Performance Formed by Metal-Induced-Lateral-Crystallization", IEDM Tech. Digest, 1999, p. 293-296.		
	AJ		Gu, J. et al., "High Performance Sub-100 nm Si Thin-Film Transistors by Pattern-Controlled Crystallization of Thin Channel Layer and High Temperature Annealing", DRC Conference Digest, 2002, pp. 49-50.		
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LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Arup Bhattacharyya	
				FILING DATE February 10, 2003	GROUP 28144
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)					
TD	AM		Feder, B.J., "I.B.M. Finds Way to Speed Up Chips", The New York Times, June 8, 2001, reprinted from		
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	AN		Rim, K. et al., "Strained Si NMOSFET's for High Performance CMOS Technology", 2001 Sympos. on VLSI Tech.		
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	AO		Li, P. et al., "Design of High Speed Si/SiGe Heterojunction Complementary MOSFETs with Reduced Short-Channel		
			Effects", Natl. Central University, ChungLi, Taiwan, ROC, Aug. 2001, Contract No. NSC 89-2215-E-008-049, National Science Council of Taiwan., pp. 1, 9.		
	AP		Ernst, T. et al., "Fabrication of a Novel Strained SiGe:C-channel Planar 55 nm nMOSFET for High-Performance		
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	AR		Belford, R.E. et al., "Performance-Augmented CMOS Using Back-End Uniaxial Strain", DRC Conf. Digest, 2002,		
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			Concentration Achieved by Ion Implantation", DRC Conf. Digest, 2002, pp. 43-44.		
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LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Arup Bhattacharyya	
				FILING DATE February 10, 2003	GROUP 281 <del>4</del>
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	AY		Tezuka, T. et al., "High-Performance Strained Si-on-Insulator MOSFETs by Novel Fabrication Processes Utilizing Ge-Condensation Technique", 2002 VLSI Tech. Digest of Technical Papers, pp. 96-97.		
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	BB		Markoff, J., "I.B.M. Circuits are Now Faster and Reduce Use of Power", The New York Times, Feb. 25, 2002; reprinted 3/20/02 from <a href="http://story.news.yahoo.com/news?tmpl=story&amp;u=/ny/20020225/...">http://story.news.yahoo.com/news?tmpl=story&amp;u=/ny/20020225/...</a> , 1 pg.		
	BC		Park, J.S. et al., "Normal Incident SiGe/Si Multiple Quantum Well Infrared Detector", IEDM Tech. Digest, 1991, pp. 749-752.		
	BD		Current, M.I. et al., "Atomic-Layer Cleaving with Si <sub>3</sub> Ge <sub>2</sub> Strain Layers for Fabrication of Si and Ge-Rich SOI Device Layers", 2001 IEEE Internatl. SOI Conf. 10/01, pp. 11-12.		
	BE		Bhattacharyya, A., "The Role of Microelectronic Integration in Environmental Control: A Perspective", Mat. Res. Soc. Symp. Proc. Vol. 344, 1994, pp. 281-293.		
	BF		Myers, S.M. et al., "Deuterium Interactions in Oxygen-Implanted Copper", J. Appl. Phys., Vol. 65(1), Jan. 1, 1989, p. 311-321.		
	BG		Saggio, M. et al., "Innovative Localized Lifetime Control in High-Speed IGBT's", IEEE Elec. Dev. Lett., V. 18, No. 7, July 1997, pp. 333-335.		
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U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
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	AF						
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FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
							Yes No
	AL						
	AM						
	AN						
	AO						
	AP						
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	AR	van Meer, H. Et al., "Ultra-Thin Film Fully-Depleted SOI CMOS with Raised G/S/D Device Architecture for Sub-100 nm Applications", 2001 IEEE Internat. SOI Conf. 10/2001, pp. 45-46.					
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